REMARKS

Entry of this amendment and reconsideration of this application as so amended is requested. By this amendment Applicant has amended the Abstract as requested by the Examiner, and has amended claim 1 for clarity. Claims 1-21 remain in the case.

The Examiner reiterated the rejection of claims 1-10 and 12-17 under 35 U.S.C. 102(b) as being anticipated by Hall, Jr. ("Hall"), and the objection to claims 11 and 18-21 as depending from a rejected base claim.

In contradistinction to Applicant's claimed invention Hall discloses an acoustic logging system for detecting and distinguishing a "shear" wave from a compression wave in response to a transmitted burst signal. A receiver 24 spaced apart from a transmitter 18 receives the compression wave before the shear wave. Lithographic information is carried by the respective velocities of the compression and shear waves and the amplitude of the compression wave. The input acoustic logging signal is sampled and stored using a sample analog delay line. A clock is used to clock out the stored samples over a longer period than the input sample period to form an expanded output. Using two receivers, the receiver nearer the transmitter is used to store peak values representing several cycles of the compression wave, which values are digitized and convolved with the digitized input acoustic logging signal from the further receiver from which the actual presence, arrival time and amplitude of the compression wave are determined.

Applicant's claimed invention is a method for high-speed synchronous digital acquisition derived in real-time from analog samples. A digital input signal includes

a clock channel and a data channel, each channel being sampled in response to a sample clock (SCLK) so that for each readout (logic) clock (LCLK) period N samples are produced. A current and prior sample for each of the N samples are compared with a threshold in a realtime Nyquist engine (RTNE) to generate for each current sample a logic level (L), an edge indicator (E) and an interpolated edge time value (TPE). The interpolated edge time value is combined with a sample time value (TPS) from the sample clock for the corresponding sample to generate bin records, with only those bins recording an edge (LEBD/LEBC) being passed on to a sample point/violation detection logic. Clock edges from the clock channel are offset and used to sample the data channel to recover the logic (digital) information.

Applicant recites in claim 1 an analog sampling array (210) for acquiring from a signal under test (SUT) a plurality of temporally offset analog samples (V_s - V_{s+n-1}) during each of a sequence of sample periods (determined by LCLK). Applicant further recites a plurality of sample processors (220) for identifying logic level transitions (transitions between logic "0" and logic "1") between respective current (V_c) and previous (V_p) samples and for determining a time of occurrence of the logic transitions (edge times). Applicant has clarified claim 1 to recite that the plurality of sample processors equals the number of the plurality of temporally offset analog samples.

The Examiner states that the Fig. 2 of Hall, which shows the signals at the respective pair of spaced-apart receivers, is an analog sampling array that acquires (as shown in Fig. 3) a signal under test (the input acoustic logging signal shown in Fig. 2) in the form of a plurality of temporally offset analog samples during each of a sequence of sample periods. A 5 ms realtime segment of the input acoustic logging

signal is sequentially sampled and stored at a 2 us sample rate to produce 2000 samples that may be stored for 500 ms. It is not clear that this analog delay line implementation is comparable to an analog sampling array. Hall does not indicate that the analog sampling is done "during each of a sequence of sample periods." The Examiner does not indicate specifically what in Hall equates to such a sequence of sample periods.

Further the Examiner states that the ADCs, RMS detector, Peak Detector and Convolver (Fig. 5) correspond to the plurality of sample processors. Claim 1 as amended recites that there is one processor for each sample within each sample period, and that each processor has as inputs respective current and previous samples in order to determine logic level transitions between such respective samples. Hall does not determine logic level transitions (i.e., changes in logic levels in a digital signal), but merely determines when a burst signal (i.e., analog signal) crosses a threshold established above an RMS ambient noise value, and then determines that the burst signal is valid by looking for a sequence of samples above the threshold with the first such sample indicating the time of the compression wave. In other words Hall is looking for the start of the compression wave or analog signal component, not for the time of occurrence of logic level or digital transitions between consecutive temporal samples.

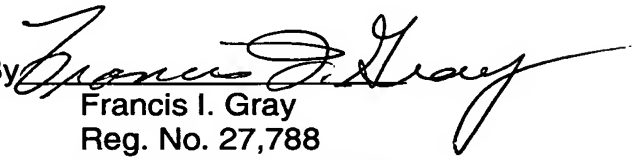
Applicant recites in claim 10 the steps of acquiring the plurality of temporally offset analog samples of the SUT during each of a sequence of sample periods, as is also recited in claim 1. Then Applicant recites determining a logic level for each sample using a threshold signal level. Hall does not establish any logic level for any samples, let alone for each sample, as Hall is not looking at a digital signal. Hall

does not generate an edge bin data structure for those samples that are at a different logic level from the immediately preceding sample. To say that the detection of a peak is the generation of an edge bin data structure is stretching the plain teaching of Hall which does not seek to establish edge bins, but merely locate the beginning of the compression wave. Also claim 10 recites an estimation of the relative threshold level crossing time of the SUT between successive samples, whereas there is no indication in Hall that such an interpolation is performed. Hall only indicates that the first sample that is above the determined noise floor is the start of the compression wave. Therefore claims 1 and 10 together with claims 2-9 and 11-21 dependent therefrom are deemed to be allowable as being neither anticipated nor rendered obvious to one of ordinary skill in the art by Hall.

In view of the foregoing amendment and remarks entry of this amendment and allowance of claims 1-21 are urged, and such action and the issuance of this case are requested.

Respectfully submitted,

GARY K. RICHMOND

By 
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